

**D546**

**ABSTRACT**

Patterned layers in an integrated circuit (IC) or other device are aligned in conjunction with the detection of the topology of the layers. The topology can be used to determine the location of a metrology mark and/or to compensate for a horizontal shift in the apparent location of the metrology mark. Precise detection of topography can be achieved without physical contact with the IC or other device with an atomic force microscope.

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